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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,214	04/01/2004	Daniel Bensahel	S1022.81113US00	7308

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EXAMINER
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RAO, G NAGESH

ART UNIT	PAPER NUMBER
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1722

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/816,214

Applicant(s)

BENSAHEL ET AL.

Examiner

G. Nagesh Rao

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 31 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) 8 and 9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

***Election/Restrictions***

1) Claims 8-9 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 7/31/06.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2) Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Tuppen (US Patent No. 5,279,687).

Tuppen 687 pertains to a method of fabricating a semiconductor device with low dislocation defects via an epitaxy process via preparing the substrates by annealing epitaxial layers in the form of mesas and substrates. Tuppen 687 includes the teachings of heterostructured monocrystalline layered devices (anticipating heteroatomic single-crystal), whereby heteroatomic refers to any element material not having hydrogen or carbon.

Tuppen 687 goes onto describe that the invention relates to the preparation of semiconductor substrate wafer one being pure Silicon and the growing of various alloy semiconductors single crystalline layers such as silicon-germanium (Col 1 Lines 5-30).

The crystal lattices of the wafer and epitaxial layer would inherently be different given the case of Si and SiGe being the respective substrate and epitaxial layer.

According to one embodiment of Tuppen 687 the Si wafer is prepared having an array of dislocations construing a roughened like surface area on the surface of the wafer prior to the epitaxial layering on top of said wafer substrate (See Col 2 Lines 8-34). This would anticipate a ring of discontinuities and with an epitaxial layer being built on top would be considered an useful region.

Tuppen 687 goes into further detail that the wafer will have a trench constructed to create channels of the sort. Said trench would be formed after the epitaxial layering (See Col 3 Lines 55-68 and Col 4 Lines 1-49). These trenches formed would allow for subsequent cutting of the wafer (See Col 6 Lines 31-50).

Tuppen 687 teaches that an additional epitaxial layer would be grown on top of the existing epitaxial layer which is built on the wafer in order to

allow for growing of microelectronic devices ontop (See Figs 1-5 (in particular Figure 2 and Claim 15)).

Furthermore Tuppen 687 teaches that dislocations which would constitute the rough areas on the wafer surface can have a range of  $10^6 - 10^{10} \text{ cm}^{-2}$  giving an average distance of .1-10 microns. Therefore anticipating the mean square deviation value of 10-30 nm as claimed by applicant.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3) Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tuppen (US Patent No. 5,279,687) in view of JP 2002-359189.

From the aforementioned Tuppen 687 teaches a single crystal solid-state device and its method of manufacturing.

However in the event Tuppen 687 is not clear to the specified teachings as claimed by applicant in claims 7. Examiner puts forth

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secondary reference JP 189 as clear indicative teachings of an additional strained Si layer placed ontop of the two-tier epitaxial layered SiGe built on said Si wafer.

Thus it would be obvious to top off the epitaxial layer with Si because one it is well known in the art and obvious to utilize in these complex single crystal solid state devices and two JP 189 suggests to top the device with Si because it would help enhance the field channel effect for a much better MOSFET device (See Figure 2 and English translation of the reference submitted for further details).


Any inquiry concerning this communication or earlier communications from the examiner should be directed to G. Nagesh Rao whose telephone number is (571) 272-2946. The examiner can normally be reached on 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta can be reached on (571)272-1316. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GNR



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